Burr-Brown Products
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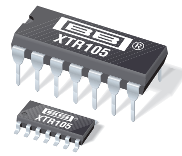
XTR105



SBOS061B – FEBRUARY 1997 – REVISED AUGUST 2004

4-20mA CURRENT TRANSMITTER with Sensor Excitation and Linearization

FEATURES

- LOW UNADJUSTED ERROR
- TWO PRECISION CURRENT SOURCES: 800μA each
- LINEARIZATION
- 2- OR 3-WIRE RTD OPERATION
- LOW OFFSET DRIFT: 0.4μV/°C
- LOW OUTPUT CURRENT NOISE: $30nA_{PP}$
- HIGH PSR: 110dB minimum
- HIGH CMR: 86dB minimum
- WIDE SUPPLY RANGE: 7.5V to 36V
- DIP-14 AND SO-14 PACKAGES

DESCRIPTION

The XTR105 is a monolithic 4-20mA, 2-wire current transmitter with two precision current sources. It provides complete current excitation for platinum RTD temperature sensors and bridges, instrumentation amplifiers, and current output circuitry on a single integrated circuit.

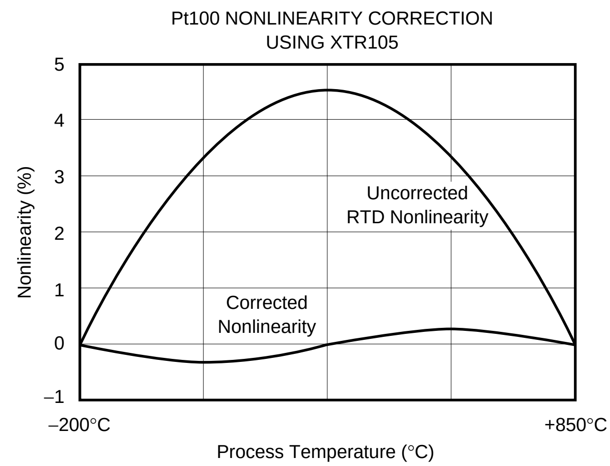
Versatile linearization circuitry provides a 2nd-order correction to the RTD, typically achieving a 40:1 improvement in linearity.

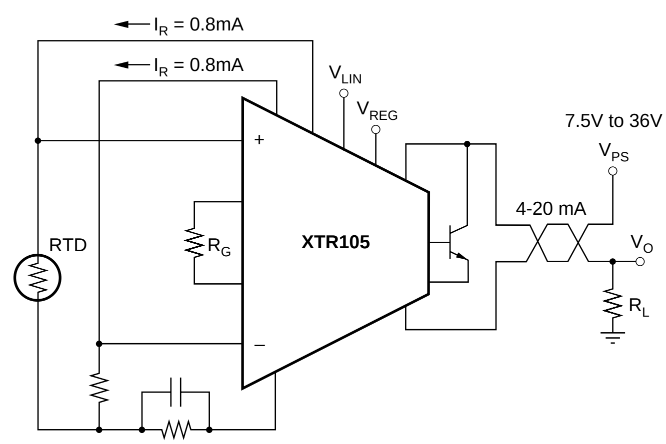
Instrumentation amplifier gain can be configured for a wide range of temperature or pressure measurements. Total unadjusted error of the complete current transmitter is low enough to permit use without adjustment in many applications. This includes zero output current drift, span drift, and nonlinearity. The XTR105 operates on loop power-supply voltages down to 7.5V.

The XTR105 is available in DIP-14 and SO-14 surface-mount packages and is specified for the –40°C to +85°C industrial temperature range.

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- SCADA REMOTE DATA ACQUISITION
- REMOTE TEMPERATURE AND PRESSURE TRANSDUCERS





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply, V+ (referenced to the I_O pin)	40V
Input Voltage, V_{IN+}, V_{IN-} (referenced to the I_O pin)	0V to V+
Storage Temperature Range	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Current Limit	Continuous
Junction Temperature	+165°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

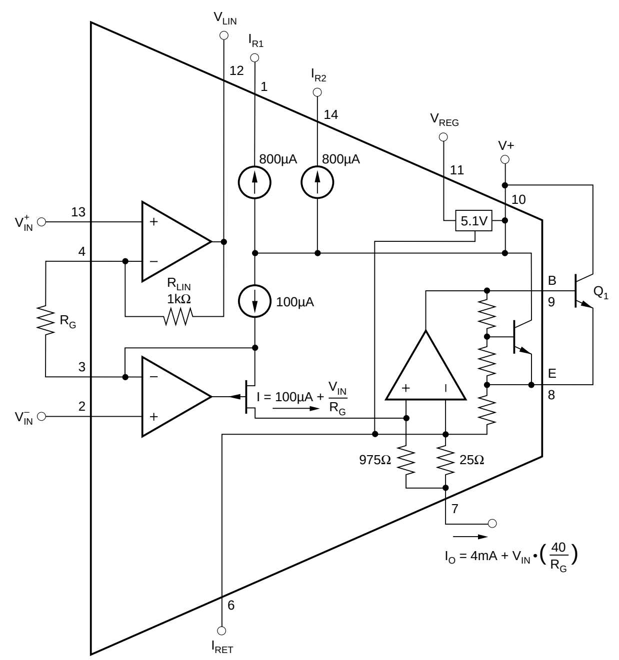
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
XTR105	DIP-14	N	–40°C to +85°C	XTR105PA	XTR105PA	Rails, 25
"	"	"	"	XTR105P	XTR105P	Rails, 25
XTR105	SO-14 Surface-Mount	D	–40°C to +85°C	XTR105UA	XTR105UA	Rails, 58
"	"	"	"	XTR105UA	XTR105UA/2K5	Tape and Reel, 2500
XTR105	SO-14 Surface-Mount	D	–40°C to +85°C	XTR105U	XTR105U	Rails, 58
"	"	"	"	XTR105U	XTR105U/2K5	Tape and Reel, 2500

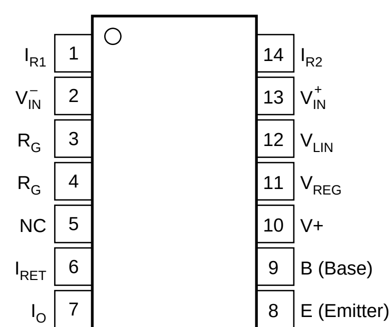
NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

Top View **DIP and SO**



NC = No Internal Connection

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V+ = 24V, and TIP29C external transistor, unless otherwise noted.

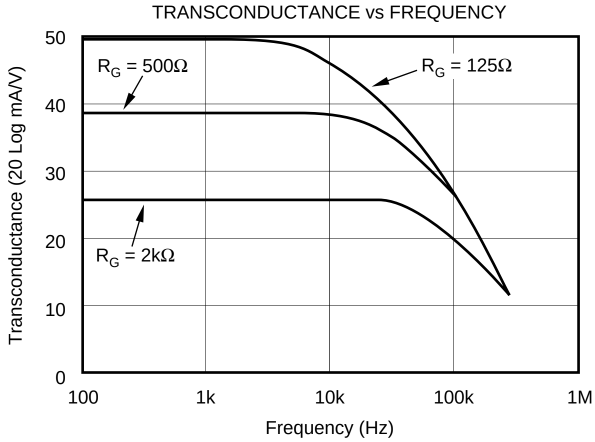
PARAMETER	CONDITIONS	XTR105P, U MIN	XTR105P, U TYP	XTR105P, U MAX	XTR105PA, UA MIN	XTR105PA, UA TYP	XTR105PA, UA MAX	UNITS
OUTPUT								
Output Current Equation		$I_O = V_{IN} \cdot (40/R_G) + 4mA$, V_{IN} in Volts, R_G in Ω						A
Output Current, Specified Range		4		20	*		*	mA
Over-Scale Limit		24	27	30	*	*	*	mA
Under-Scale Limit	I_{REG} = 0V	1.8	2.2	2.6	*	*	*	mA
ZERO OUTPUT(1)	V_{IN} = 0V, R_G = ∞		4			*		mA
Initial Error			±5	±25		*	±50	µA
vs Temperature			±0.07	±0.5		*	±0.9	µA/°C
vs Supply Voltage, V+	V+ = 7.5V to 36V		0.04	0.2		*	*	µA/V
vs Common-Mode Voltage	V_{CM} = 1.25V to 3.5V(2)		0.02			*		µA/V
vs V_{REG} Output Current			0.3			*		µA/mA
Noise, 0.1Hz to 10Hz			0.03			*		$µA_{PP}$
SPAN								
Span Equation (transconductance)			S = $40/R_G$			*		A/V
Initial Error (3)	Full-Scale (V_{IN}) = 50mV		±0.05	±0.2		*	±0.4	%
vs Temperature(3)			±3	±25		*	*	ppm/°C
Nonlinearity, Ideal Input (4)	Full-Scale (V_{IN}) = 50mV		0.003	0.01		*	*	%
INPUT(5)								
Offset Voltage	V_{CM} = 2V		±50	±100		*	±250	µV
vs Temperature			±0.4	±1.5		*	±3	µV/°C
vs Supply Voltage, V+	V+ = 7.5V to 36V		±0.3	±3		*	*	µV/V
vs Common-Mode Voltage, RTI (CMRR)	V_{CM} = 1.25V to 3.5V(2)		±10	±50		*	±100	µV/V
Common-Mode Input Range(2)		1.25		3.5	*		*	V
Input Bias Current			5	25		*	50	nA
vs Temperature			20			*		pA/°C
Input Offset Current			±0.2	±3		*	±10	nA
vs Temperature			5			*		pA/°C
Impedance, Differential			0.1 || 1			*		GΩ || pF
Common-Mode			5 || 10			*		GΩ || pF
Noise, 0.1Hz to 10Hz			0.6			*		$µV_{PP}$
CURRENT SOURCES	V_O = 2V(6)							
Current			800			*		µA
Accuracy			±0.05	±0.2		*	±0.4	%
vs Temperature			±15	±35		*	±75	ppm/°C
vs Power Supply, V+	V+ = 7.5V to 36V		±10	±25		*	*	ppm/V
Matching			±0.02	±0.1		*	±0.2	%
vs Temperature			±3	±15		*	±30	ppm/°C
vs Power Supply, V+	V+ = 7.5V to 36V		1	10		*	*	ppm/V
Compliance Voltage, Positive		(V+) – 3	(V+) – 2.5		*	*		V
Negative(2)		0	–0.2		*	*		V
Output Impedance			150			*		MΩ
Noise, 0.1Hz to 10Hz			0.003			*		$µA_{PP}$
V_{REG}(2)			5.1			*		V
Accuracy			±0.02	±0.1		*	*	V
vs Temperature			±0.2			*		mV/°C
vs Supply Voltage, V+			1			*		mV/V
Output Current			±1			*		mA
Output Impedance			75			*		Ω
LINEARIZATION								
R_{LIN} (internal)			1			*		kΩ
Accuracy			±0.2	±0.5		*	±1	%
vs Temperature			±25	±100		*	*	ppm/°C
POWER SUPPLY								
Specified			+24			*		V
Voltage Range		+7.5		+36	*		*	V
TEMPERATURE RANGE								
Specification, T_{MIN} to T_{MAX}		–40		+85	*		*	°C
Operating		–55		+125	*		*	°C
Storage		–55		+125	*		*	°C
Thermal Resistance, θ_{JA}								
DIP-14			80			*		°C/W
SO-14 Surface-Mount			100			*		°C/W

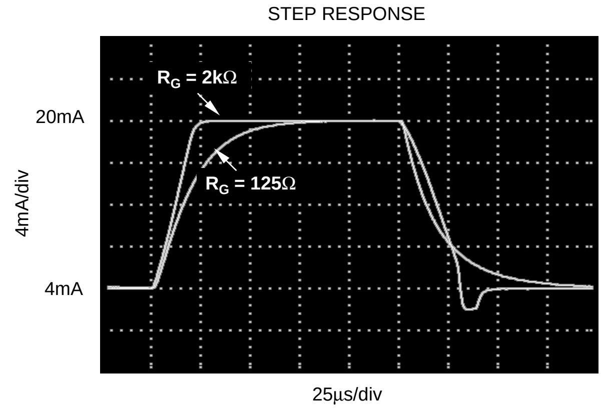
* Specification same as XTR105P and XTR105U.

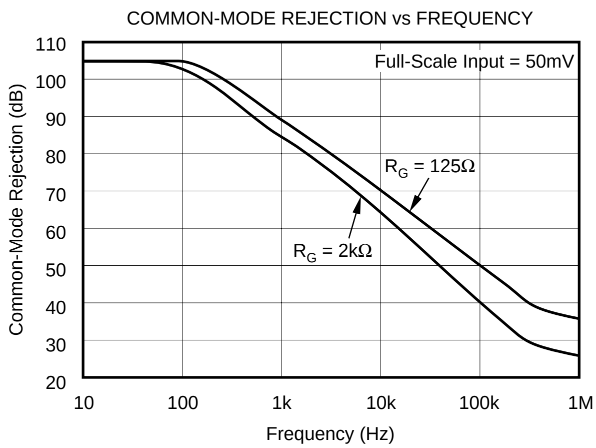
NOTES: (1) Describes accuracy of the 4mA low-scale offset current. Does not include input amplifier effects. Can be trimmed to zero.
(2) Voltage measured with respect to I_{RET} pin.
(3) Does not include initial error or TCR of gain-setting resistor, R_G.
(4) Increasing the full-scale input range improves nonlinearity.
(5) Does not include Zero Output initial error.
(6) Current source output voltage with respect to I_{RET} pin.

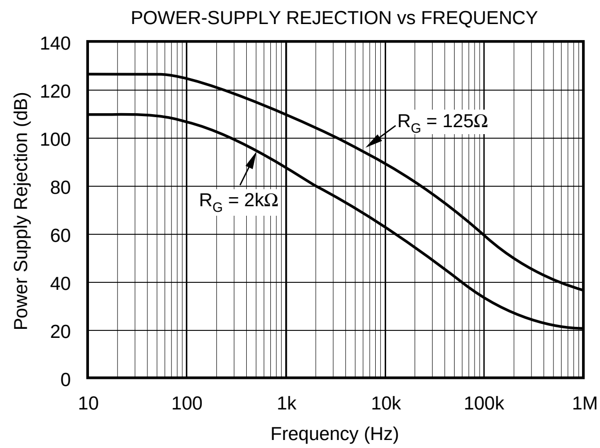
TYPICAL CHARACTERISTICS

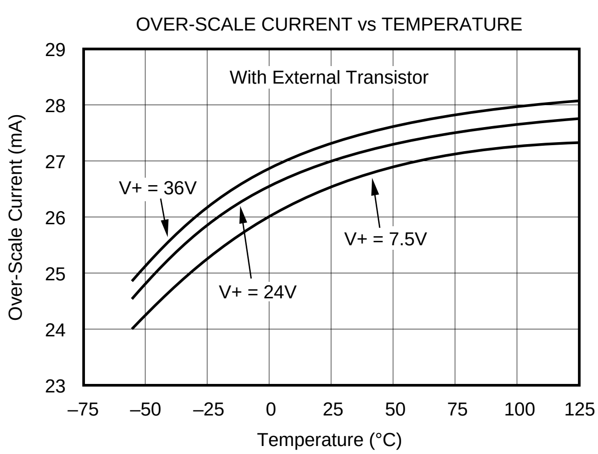
At $T_A = +25°C$ and V+ = 24V, unless otherwise noted.

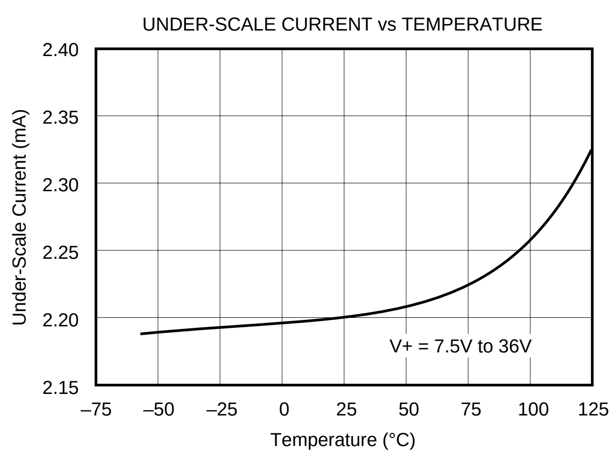






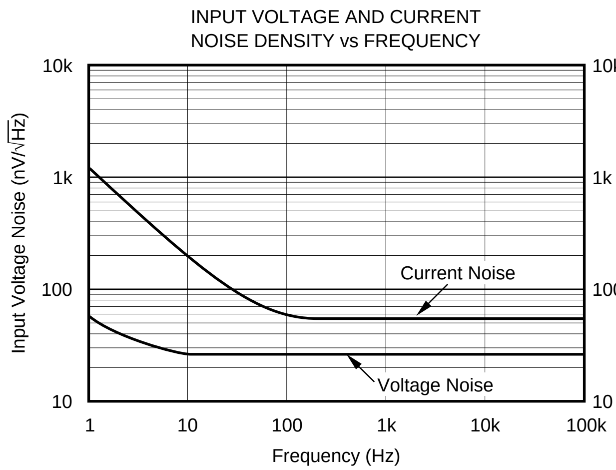


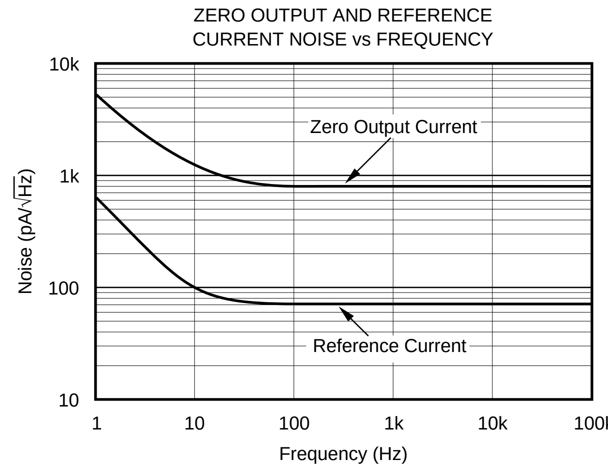


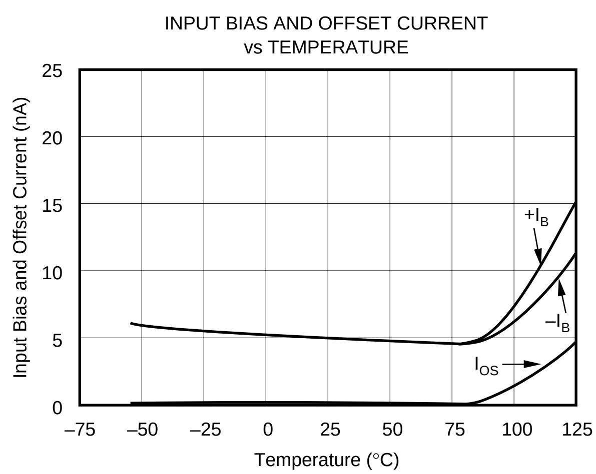


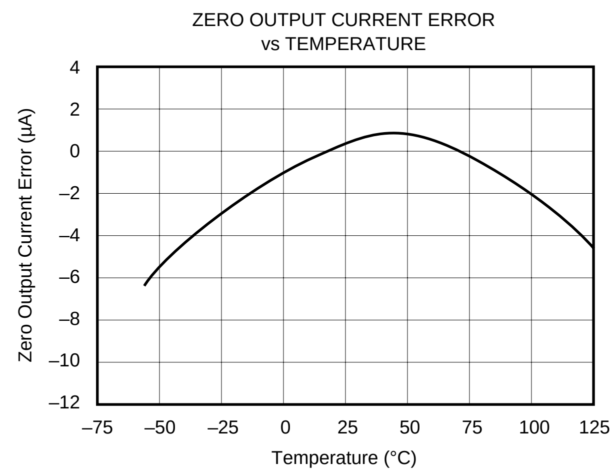
TYPICAL CHARACTERISTICS (Cont.)

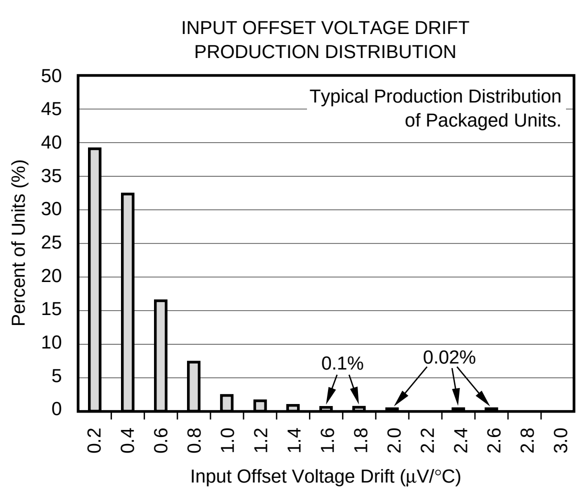
At $T_A = +25°C$ and V+ = 24V, unless otherwise noted.

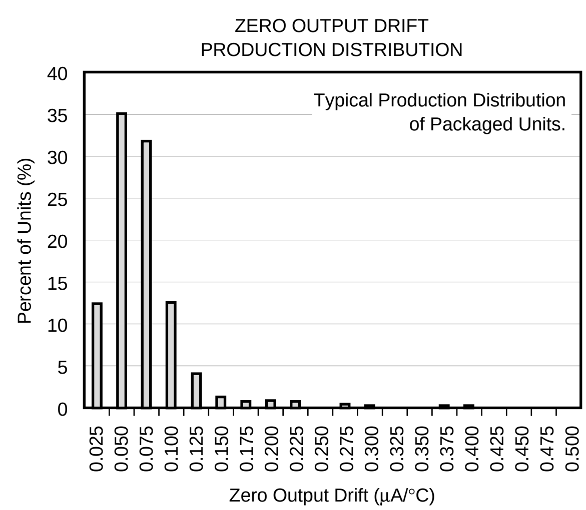






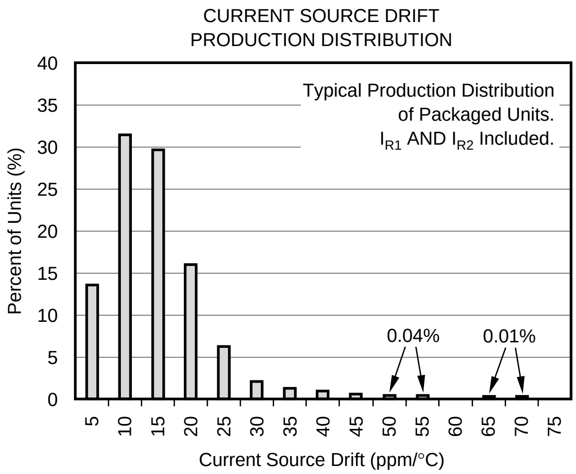


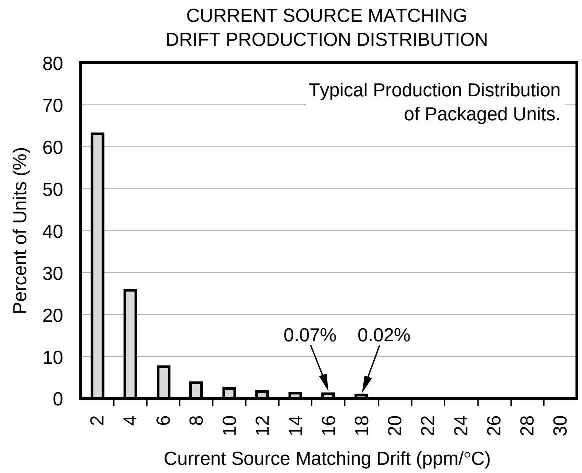


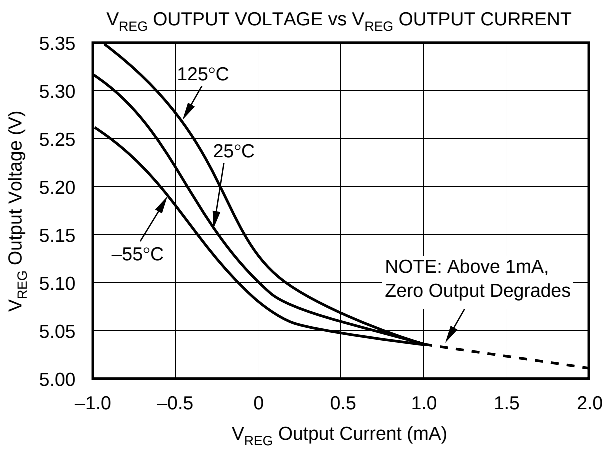


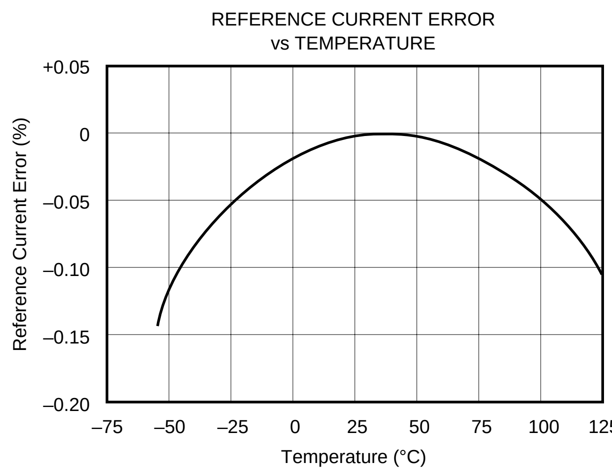
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C and V+ = 24V, unless otherwise noted.









APPLICATION INFORMATION

Figure 1 shows the basic connection diagram for the XTR105. The loop power supply, V_{PS}, provides power for all circuitry. Output loop current is measured as a voltage across the series load resistor, R_L.

Two matched 0.8mA current sources drive the RTD and zero-setting resistor, R_Z. The instrumentation amplifier input of the XTR105 measures the voltage difference between the RTD and R_Z. The value of R_Z is chosen to be equal to the resistance of the RTD at the low-scale (minimum) measurement temperature. R_Z can be adjusted to achieve 4mA output at the minimum measurement temperature to correct for input offset voltage and reference current mismatch of the XTR105.

R_{CM} provides an additional voltage drop to bias the inputs of the XTR105 within their common-mode input range. R_{CM} should be bypassed with a 0.01µF capacitor to minimize common-mode noise. Resistor R_G sets the gain of the instrumentation amplifier according to the desired temperature range. R_{LIN1} provides 2nd-order linearization correction to the RTD, typically achieving a 40:1 improvement in linearity. An additional resistor is required for 3-wire RTD connections (see Figure 3).

The transfer function through the complete instrumentation amplifier and voltage-to-current converter is:

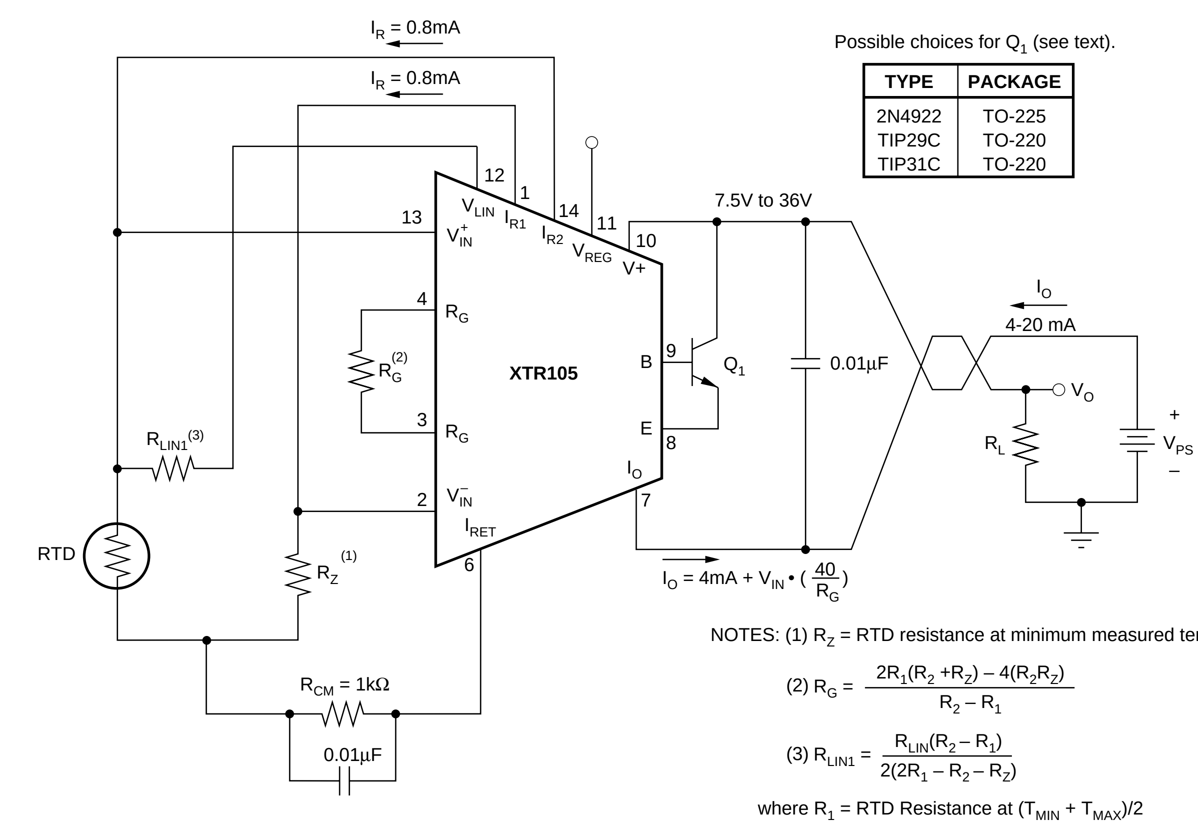
$$I_O = 4mA + V_{IN} \bullet (40/R_G)$$
$$(V_{IN} \text{ in volts, } R_G \text{ in ohms})$$

where V_{IN} is the differential input voltage.

As evident from the transfer function, if no R_G is used the gain is zero and the output is simply the XTR105's zero current. The value of R_G varies slightly for 2-wire RTD and 3-wire RTD connections with linearization. R_G can be calculated from the equations given in Figure 1 (2-wire RTD connection) and Table I (3-wire RTD connection).

The I_{RET} pin is the return path for all current from the current sources and V_{REG}. The I_{RET} pin allows any current used in external circuitry to be sensed by the XTR105 and to be included in the output current without causing an error.

The V_{REG} pin provides an on-chip voltage source of approximately 5.1V and is suitable for powering external input circuitry (refer to Figure 6). It is a moderately accurate voltage reference—it is not the same reference used to set the 800µA current references. V_{REG} is capable of sourcing approximately 1mA of current. Exceeding 1mA may affect the 4mA zero output.



Possible choices for Q_1 (see text).

TYPE	PACKAGE
2N4922	TO-225
TIP29C	TO-220
TIP31C	TO-220

NOTES: (1) R_Z = RTD resistance at minimum measured temperature.

(2) $R_G = \dfrac{2R_1(R_2 + R_Z) - 4(R_2 R_Z)}{R_2 - R_1}$

(3) $R_{LIN1} = \dfrac{R_{LIN}(R_2 - R_1)}{2(2R_1 - R_2 - R_Z)}$

where R_1 = RTD Resistance at $(T_{MIN} + T_{MAX})/2$

R_2 = RTD Resistance at T_{MAX}

R_{LIN} = 1kΩ (Internal)

FIGURE 1. Basic 2-Wire RTD Temperature Measurement Circuit with Linearization.

MEASUREMENT TEMPERATURE SPAN ΔT (°C)

T_{MIN}	100°C	200°C	300°C	400°C	500°C	600°C	700°C	800°C	900°C	1000°C
–200°C	18.7/86.6 15000 16500	18.7/169 9760 11500	18.7/255 8060 10000	18.7/340 6650 8870	18.7/422 5620 7870	18.7/511 4750 7150	18.7/590 4020 6420	18.7/665 3480 5900	18.7/750 3090 5360	18.7/845 2740 4990
–100°C	60.4/80.6 27400 29400	60.4/162 15400 17800	60.4/243 10500 13000	60.4/324 7870 10200	60.4/402 6040 8660	60.4/487 4990 7500	60.4/562 4220 6490	60.4/649 3570 5900	60.4/732 3090 5360	
0°C	100/78.7 33200 35700	100/158 16200 18700	100/237 10500 13000	100/316 7680 10000	100/392 6040 8250	100/475 4870 7150	100/549 4020 6340	100/634 3480 5620		
100°C	137/75 31600 34000	137/150 15400 17800	137/226 10200 12400	137/301 7500 9760	137/383 5760 8060	137/453 4750 6810	137/536 3920 6040			
200°C	174/73.2 30900 33200	174/147 15000 17400	174/221 9760 12100	174/294 7150 9310	174/365 5620 7680	174/442 4530 6490				
300°C	210/71.5 30100 32400	210/143 14700 16500	210/215 9530 11500	210/287 6980 8870	210/357 5360 7320					
400°C	249/68.1 28700 30900	249/137 14000 16200	249/205 9090 11000	249/274 6650 8450						
500°C	280/66.5 28000 30100	280/133 13700 15400	280/200 8870 10500							
600°C	316/64.9 26700 28700	313/130 13000 14700								
700°C	348/61.9 26100 27400									
800°C	374/60.4 24900 26700									

R_Z / R_G
R_{LIN1}
R_{LIN2}

NOTE: The values listed in this table are 1% resistors (in Ω). Exact values may be calculated from the following equations:

R_Z = RTD resistance at minimum measured temperature.

$$R_G = \frac{2(R_2 - R_Z)(R_1 - R_Z)}{(R_2 - R_1)}$$

$$R_{LIN1} = \frac{R_{LIN}(R_2 - R_1)}{2(2R_1 - R_2 - R_Z)}$$

$$R_{LIN2} = \frac{(R_{LIN} + R_G)(R_2 - R_1)}{2(2R_1 - R_2 - R_Z)}$$

where: R_1 = RTD resistance at $(T_{MIN} + T_{MAX})/2$
R_2 = RTD resistance at T_{MAX}
R_{LIN} = 1kΩ (Internal)

EXAMPLE:

The measurement range is –100°C to +200°C for a 3-wire Pt100 RTD connection. Determine the values for R_S, R_G, R_{LIN1}, and R_{LIN2}. Look up the values from the chart or calculate the values according to the equations provided.

METHOD 1: TABLE LOOK UP

For T_{MIN} = –100°C and ΔT = –300°C, the 1% values are:

R_Z = 60.4Ω R_{LIN1} = 10.5kΩ
R_G = 243Ω R_{LIN2} = 13kΩ

METHOD 2: CALCULATION

Step 1: Determine R_Z, R_1, and R_2.

R_Z is the RTD resistance at the minimum measured temperature, T_{MIN} = –100°C. Using Equation 1 at right gives R_Z = 60.25Ω (1% value is 60.4Ω).

R_2 is the RTD resistance at the maximum measured temperature, T_{MAX} = 200°C. Using Equation 2 at right gives R_2 = 175.84Ω.

R_1 is the RTD resistance at the midpoint measured temperature, $T_{MID} = (T_{MIN} + T_{MAX})/2$ = 50°C. R_1 is NOT the average of R_Z and R_2. Using Equation 2 at right gives R_1 = 119.40Ω.

Step 2: Calculate R_G, R_{LIN1}, and R_{LIN2} using equations above.

R_G = 242.3Ω (1% value is 243Ω)
R_{LIN1} = 10.413kΩ (1% value is 10.5kΩ)
R_{LIN2} = 12.936kΩ (1% value is 13kΩ)

Calculation of Pt100 Resistance Values
(according to DIN IEC 751)

(Equation 1) Temperature range from –200°C to 0°C:
$R_{(T)} = 100\ [1 + 3.90802 \cdot 10^{-3} \cdot T - 0.5802 \cdot 10^{-6} \cdot T^2 - 4.27350 \cdot 10^{-12}\ (T - 100)\ T^3]$

(Equation 2) Temperature range from 0°C to +850°C:
$R_{(T)} = 100\ (1 + 3.90802 \cdot 10^{-3} \cdot T - 0.5802 \cdot 10^{-6} \cdot T_2)$

where: $R_{(T)}$ is the resistance in Ω at temperature T.
T is the temperature in °C.

NOTE: Most RTD manufacturers provide reference tables for resistance values at various temperatures.

TABLE I. R_Z, R_G, R_{LIN1}, and R_{LIN2} Standard 1% Resistor Values for 3-Wire Pt100 RTD Connection with Linearization.

A negative input voltage, V_{IN}, will cause the output current to be less than 4mA. Increasingly negative V_{IN} will cause the output current to limit at approximately 2.2mA. Refer to the typical characteristic Under-Scale Current vs Temperature.

Increasingly positive input voltage (greater than the full-scale input) will produce increasing output current according to the transfer function, up to the output current limit of approximately 27mA. Refer to the typical characteristic Over-Scale Current vs Temperature.

EXTERNAL TRANSISTOR

Transistor Q_1 conducts the majority of the signal-dependent 4-20mA loop current. Using an external transistor isolates the majority of the power dissipation from the precision input and reference circuitry of the XTR105, maintaining excellent accuracy.

Since the external transistor is inside a feedback loop, its characteristics are not critical. Requirements are: V_{CEO} = 45V min, β = 40 min, and P_D = 800mW. Power dissipation requirements may be lower if the loop power-supply voltage is less than 36V. Some possible choices for Q_1 are listed in Figure 1.

The XTR105 can be operated without this external transistor, however, accuracy will be somewhat degraded due to the internal power dissipation. Operation without Q_1 is not recommended for extended temperature ranges. A resistor (R = 3.3kΩ) connected between the I_{RET} pin and the E (emitter) pin may be needed for operation below 0°C without Q_1 to ensure the full 20mA full-scale output, especially with V+ near 7.5V.

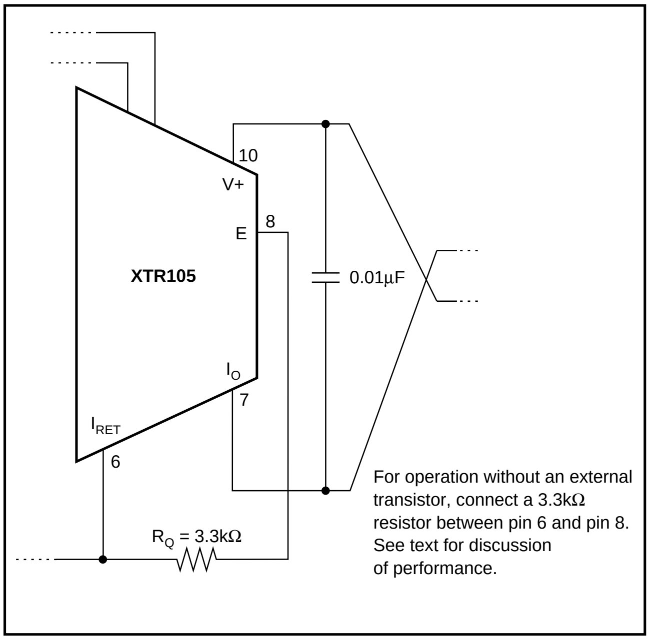


FIGURE 2. Operation Without an External Transistor.

LOOP POWER SUPPLY

The voltage applied to the XTR105, V+, is measured with respect to the I_O connection, pin 7. V+ can range from 7.5V to 36V. The loop-supply voltage, V_{PS}, will differ from the voltage applied to the XTR105 according to the voltage drop on the current sensing resistor, R_L (plus any other voltage drop in the line).

If a low loop-supply voltage is used, R_L (including the loop wiring resistance) must be made a relatively low value to assure that V+ remains 7.5V or greater for the maximum loop current of 20mA:

$$R_L \max = \left(\frac{(V+) - 7.5V}{20mA}\right) - R_{WIRING}$$

It is recommended to design for V+ equal or greater than 7.5V with loop currents up to 30mA to allow for out-of-range input conditions.

The low operating voltage (7.5V) of the XTR105 allows operation directly from personal computer power supplies (12V ±5%). When used with the RCV420 current loop receiver (see Figure 7), the load resistor voltage drop is limited to 3V.

ADJUSTING INITIAL ERRORS

Many applications require adjustment of initial errors. Input offset and reference current mismatch errors can be corrected by adjustment of the zero resistor, R_Z. Adjusting the gain-setting resistor, R_G, corrects any errors associated with gain.

2- AND 3-WIRE RTD CONNECTIONS

In Figure 1, the RTD can be located remotely simply by extending the two connections to the RTD. With this remote 2-wire connection to the RTD, line resistance will introduce error. This error can be partially corrected by adjusting the values of R_Z, R_G, and R_{LIN1}.

A better method for remotely located RTDs is the 3-wire RTD connection (see Figure 3). This circuit offers improved accuracy. R_Z's current is routed through a third wire to the RTD. Assuming line resistance is equal in RTD lines 1 and 2, this produces a small common-mode voltage that is rejected by the XTR105. A second resistor, R_{LIN2}, is required for linearization.

Note that although the 2-wire and 3-wire RTD connection circuits are very similar, the gain-setting resistor, R_G, has slightly different equations:

2-wire: $$R_G = \frac{2R_1(R_2 + R_Z) - 4(R_2R_Z)}{R_2 - R_1}$$

3-wire: $$R_G = \frac{2(R_2 - R_Z)(R_1 - R_Z)}{R_2 - R_1}$$

where: R_Z = RTD resistance at T_{MIN}

R_1 = RTD resistance at $(T_{MIN} + T_{MAX})/2$

R_2 = RTD resistance at T_{MAX}

To maintain good accuracy, at least 1% (or better) resistors should be used for R_G. Table I provides standard 1% R_G resistor values for a 3-wire Pt100 RTD connection with linearization.

LINEARIZATION

RTD temperature sensors are inherently (but predictably) nonlinear. With the addition of one or two external resistors, R_{LIN1} and R_{LIN2}, it is possible to compensate for most of this nonlinearity resulting in 40:1 improvement in linearity over the uncompensated output.

See Figure 1 for a typical 2-wire RTD application with linearization. Resistor R_{LIN1} provides positive feedback and controls linearity correction. R_{LIN1} is chosen according to the desired temperature range. An equation is given in Figure 1.

In 3-wire RTD connections, an additional resistor, R_{LIN2}, is required. As with the 2-wire RTD application, R_{LIN1} provides positive feedback for linearization. R_{LIN2} provides an offset canceling current to compensate for wiring resistance encountered in remotely located RTDs. R_{LIN1} and R_{LIN2} are chosen such that their currents are equal. This makes the voltage drop in the wiring resistance to the RTD a common-mode signal that is rejected by the XTR105. The nearest standard 1% resistor values for R_{LIN1} and R_{LIN2} should be adequate for most applications. Table I provides the 1% resistor values for a 3-wire Pt100 RTD connection.

If no linearity correction is desired, the V_{LIN} pin should be left open. With no linearization, $R_G = 2500 \cdot V_{FS}$, where V_{FS} = full-scale input range.

RTDs

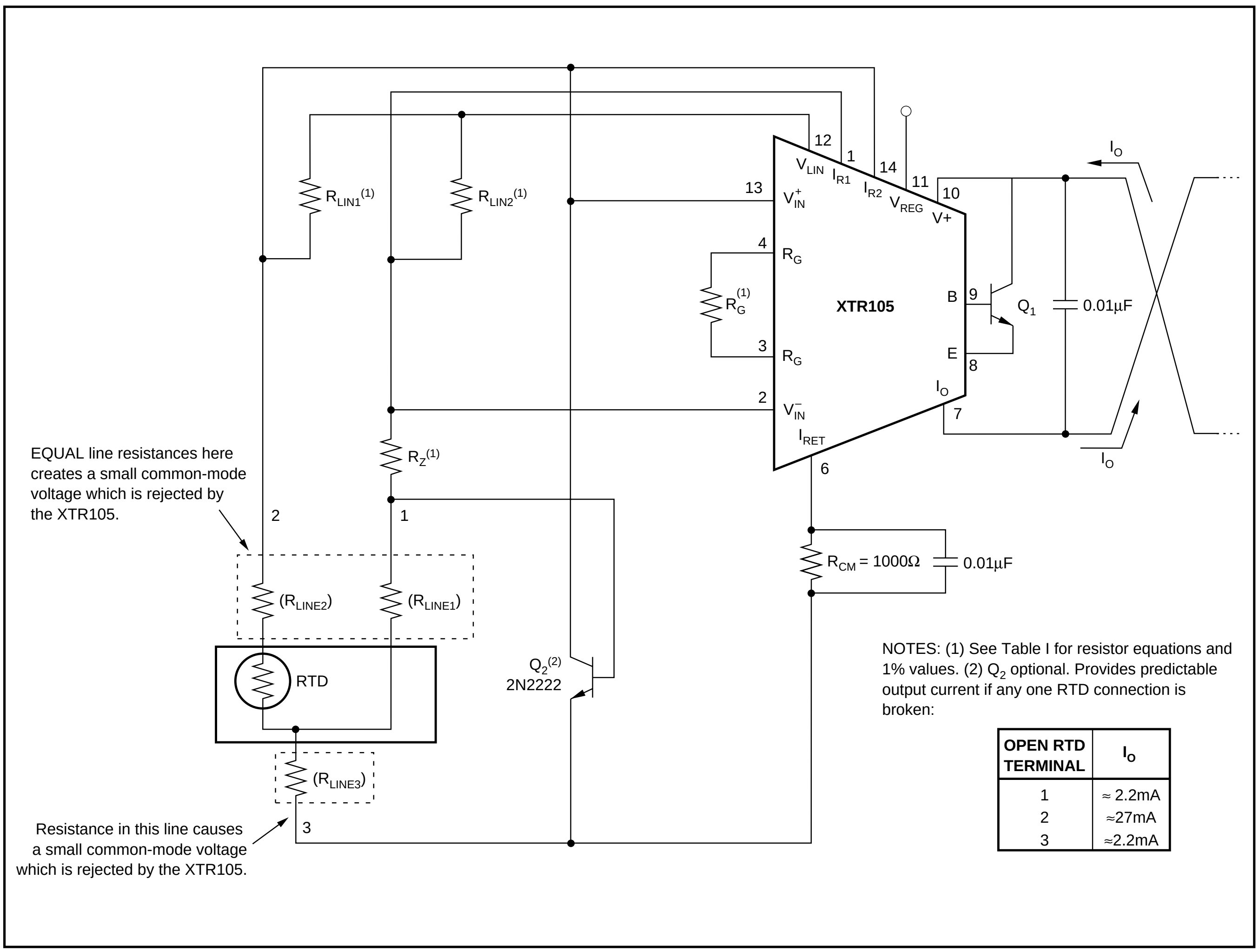
The text and figures thus far have assumed a Pt100 RTD. With higher resistance RTDs, the temperature range and input voltage variation should be evaluated to ensure proper common-mode biasing of the inputs. As mentioned earlier, R_{CM} can be adjusted to provide an additional voltage drop to bias the inputs of the XTR105 within their common-mode input range.

ERROR ANALYSIS

See Table II for how to calculate the effect various error sources have on circuit accuracy. A sample error calculation for a typical RTD measurement circuit (Pt100 RTD, 200°C measurement span) is provided. The results reveal the XTR105's excellent accuracy, in this case 1.1% unadjusted. Adjusting resistors R_G and R_Z for gain and offset errors improves circuit accuracy to 0.32%. Note that these are worst-case errors; ensured maximum values were used in the calculations and all errors were assumed to be positive (additive). The XTR105 achieves performance that is difficult to obtain with discrete circuitry and requires less space.

OPEN-CIRCUIT PROTECTION

The optional transistor Q_2 in Figure 3 provides predictable behavior with open-circuit RTD connections. It assures that if any one of the three RTD connections is broken, the XTR105's output current will go to either its high current limit (≈ 27mA) or low current limit (≈ 2.2mA). This is easily detected as an out-of-range condition.



OPEN RTD TERMINAL	I_O
1	≈ 2.2mA
2	≈27mA
3	≈2.2mA

FIGURE 3. Remotely Located RTDs with 3-Wire Connection.

SAMPLE ERROR CALCULATION

RTD value at 4mA Output ($R_{RTD\ MIN}$): 100Ω
RTD Measurement Range: 200°C
Ambient Temperature Range (ΔT_A): 20°C
Supply Voltage Change (ΔV+): 5V
Common-Mode Voltage Change (ΔCM): 0.1V

ERROR SOURCE	ERROR EQUATION	SAMPLE ERROR CALCULATION(1)	ERROR (ppm of Full Scale) UNADJ.	ERROR (ppm of Full Scale) ADJUST.
INPUT				
Input Offset Voltage	$V_{OS}/(V_{IN\ MAX}) \cdot 10^6$	$100\mu V/(800\mu A \cdot 0.38\Omega/°C \cdot 200°C) \cdot 10^6$	1645	0
vs Common-Mode	$CMRR \cdot \Delta CM/(V_{IN\ MAX}) \cdot 10^6$	$50\mu V/V \cdot 0.1V/(800\mu A \cdot 0.38\Omega/°C \cdot 200°C) \cdot 10^6$	82	82
Input Bias Current	$I_B/I_{REF} \cdot 10^6$	$0.025\mu A/800\mu A \cdot 10^6$	31	0
Input Offset Current	$I_{OS} \cdot R_{RTD\ MIN}/(V_{IN\ MAX}) \cdot 10^6$	$3nA \cdot 100\Omega/(800\mu A \cdot 0.38\Omega/°C \cdot 200°C) \cdot 10^6$	5	0
		Total Input Error:	**1763**	**82**
EXCITATION				
Current Reference Accuracy	I_{REF} Accuracy (%)/100% • 10^6	$0.2\%/100\% \cdot 10^6$	2000	0
vs Supply	$(I_{REF}$ vs V+) • ΔV+	25ppm/V • 5V	125	125
Current Reference Matching	I_{REF} Matching (%)/100% • 800µA • $R_{RTD\ MIN}/(V_{IN\ MAX}) \cdot 10^6$	$0.1\%/100\% \cdot 800\mu A \cdot 100\Omega/(800\mu A \cdot 0.38\Omega/°C \cdot 200°C) \cdot 10^6$	1316	0
vs Supply	$(I_{REF}$ Matching vs V+) • ΔV+ • $R_{RTD\ MIN}/(V_{IN\ MAX})$	$10ppm/V \cdot 5V \cdot 800\mu A \cdot 100\Omega/(800\mu A \cdot 0.38\Omega/°C \cdot 200°C)$	66	66
		Total Excitation Error:	**3507**	**191**
GAIN				
Span	Span Error (%)/100% • 10^6	$0.2\%/100\% \cdot 10^6$	2000	0
Nonlinearity	Nonlinearity (%)/100% • 10^6	$0.01\%/100\% \cdot 10^6$	100	100
		Total Gain Error:	**2100**	**100**
OUTPUT				
Zero Output	$(I_{ZERO} - 4mA)/16000\mu A \cdot 10^6$	$25\mu A/16000\mu A \cdot 10^6$	1563	0
vs Supply	$(I_{ZERO}$ vs V+) • ΔV+/16000µA • 10^6	$0.2\mu A/V \cdot 5V/16000\mu A \cdot 10^6$	63	63
		Total Output Error:	**1626**	**63**
DRIFT (ΔT_A = 20°C)				
Input Offset Voltage	Drift • $\Delta T_A/(V_{IN\ MAX}) \cdot 10^6$	$1.5\mu V/°C \cdot 20°C/(800\mu A \cdot 0.38\Omega/°C \cdot 200°C) \cdot 10^6$	493	493
Input Bias Current (typical)	Drift • $\Delta T_A/800\mu A \cdot 10^6$	$20pA/°C \cdot 20°C/800\mu A \cdot 10^6$	0.5	0.5
Input Offset Current (typical)	Drift • $\Delta T_A \cdot R_{RTD\ MIN}/(V_{IN\ MAX}) \cdot 10^6$	$5pA/°C \cdot 20°C \cdot 100W/(800\mu A \cdot 0.38\Omega/°C \cdot 200°C) \cdot 10^6$	0.2	0.2
Current Reference Accuracy	Drift • ΔT_A	35ppm/°C • 20°C	700	700
Current Reference Matching	Drift • $\Delta T_A \cdot 800\mu A \cdot R_{RTD\ MIN}/(V_{IN\ MAX})$	$15ppm/°C \cdot 20°C \cdot 800\mu A \cdot 100\Omega/(800\mu A \cdot 0.38\Omega/°C \cdot 200°C)$	395	395
Span	Drift • ΔT_A	25ppm/°C • 20°C	500	500
Zero Output	Drift • $\Delta T_A/16000\mu A \cdot 10^6$	$0.5\mu A/°C \cdot 20°C/16000\mu A \cdot 10^6$	626	626
		Total Drift Error:	**2715**	**2715**
NOISE (0.1Hz to 10Hz, typ)				
Input Offset Voltage	$v_n/(V_{IN\ MAX}) \cdot 10^6$	$0.6\mu V/(800\mu A \cdot 0.38\Omega/°C \cdot 200°C) \cdot 10^6$	10	10
Current Reference	I_{REF} Noise • $R_{RTD\ MIN}/(V_{IN\ MAX}) \cdot 10^6$	$3nA \cdot 100\Omega/(800\mu A \cdot 0.38\Omega/°C \cdot 200°C) \cdot 10^6$	5	5
Zero Output	I_{ZERO} Noise/16000µA • 10^6	$0.03\mu A/16000\mu A \cdot 10^6$	2	2
		Total Noise Error:	**17**	**17**
		TOTAL ERROR:	**11728 (1.17%)**	**3168 (0.32%)**

NOTE (1): All errors are min/max and referred to input unless otherwise stated.

TABLE II. Error Calculation.

REVERSE-VOLTAGE PROTECTION

The XTR105's low compliance rating (7.5V) permits the use of various voltage protection methods without compromising operating range. Figure 4 shows a diode bridge circuit that allows normal operation even when the voltage connection lines are reversed. The bridge causes a two diode drop (approximately 1.4V) loss in loop-supply voltage. This results in a compliance voltage of approximately 9V—satisfactory for most applications. If a 1.4V drop in loop supply is too much, a diode can be inserted in series with the loop-supply voltage and the V+ pin. This protects against reverse output connection lines with only a 0.7V loss in loop-supply voltage.

SURGE PROTECTION

Remote connections to current transmitters can sometimes be subjected to voltage surges. It is prudent to limit the maximum surge voltage applied to the XTR105 to as low as practical. Various zener diodes and surge clamping diodes are specially designed for this purpose. Select a clamp diode with as low a voltage rating as possible for best protection. For example, a 36V protection diode will assure proper transmitter operation at normal loop voltages, yet will provide an appropriate level of protection against voltage surges. Characterization tests on three production lots showed no damage to the XTR105 within loop-supply voltages up to 65V.

Most surge protection zener diodes have a diode characteristic in the forward direction that will conduct excessive current, possibly damaging receiving-side circuitry if the loop connections are reversed. If a surge protection diode is used, a series diode or diode bridge should be used for protection against reversed connections.

RADIO FREQUENCY INTERFERENCE

The long wire lengths of current loops invite radio frequency (RF) interference. RF can be rectified by the sensitive input circuitry of the XTR105 causing errors. This generally appears as an unstable output current that varies with the position of loop supply or input wiring.

If the RTD sensor is remotely located, the interference may enter at the input terminals. For integrated transmitter assemblies with short connections to the sensor, the interference more likely comes from the current loop connections.

Bypass capacitors on the input reduce or eliminate this input interference. Connect these bypass capacitors to the I_{RET} terminal (see Figure 5). Although the dc voltage at the I_{RET} terminal is not equal to 0V (at the loop supply, V_{PS}), this circuit point can be considered the transmitter's "ground." The 0.01µF capacitor connected between V+ and I_O may help minimize output interference.

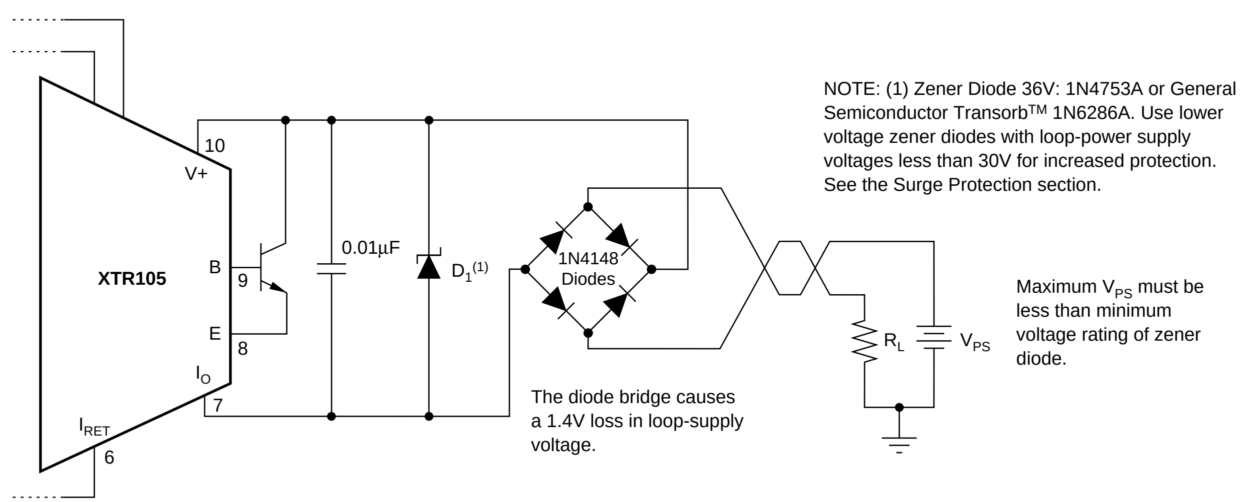


FIGURE 4. Reverse Voltage Operation and Over-Voltage Surge Protection.

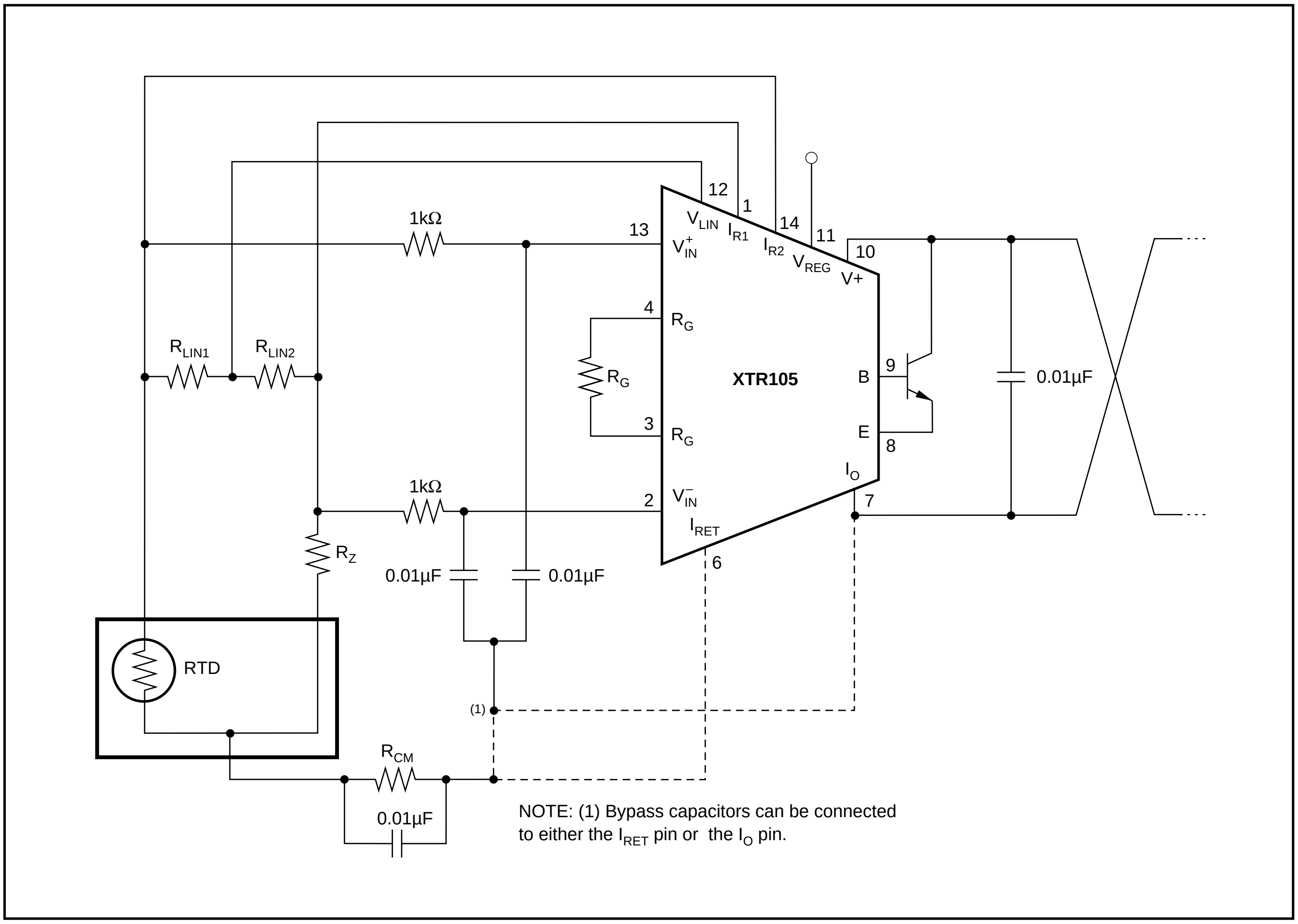


FIGURE 5. Input Bypassing Technique with Linearization.

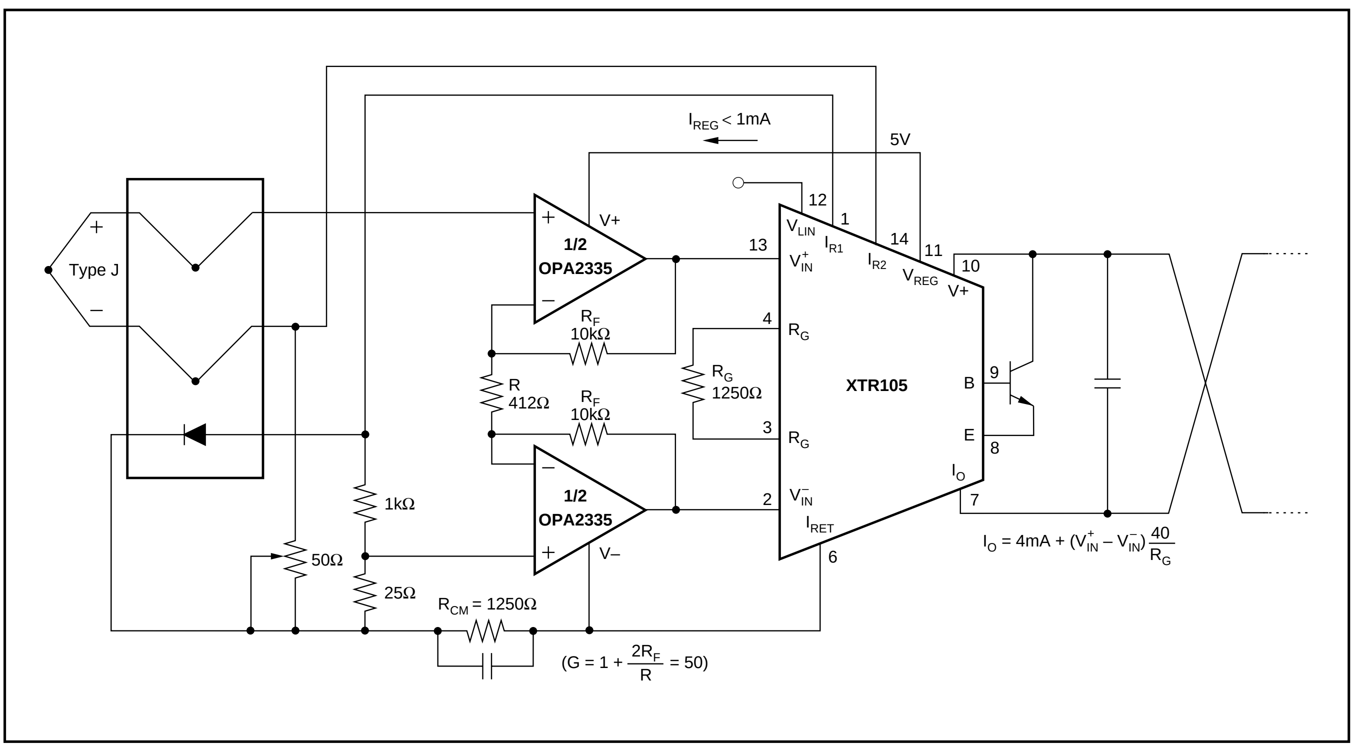


FIGURE 6. Thermocouple Low Offset, Low Drift Loop Measurement with Diode Cold Junction Compensation.

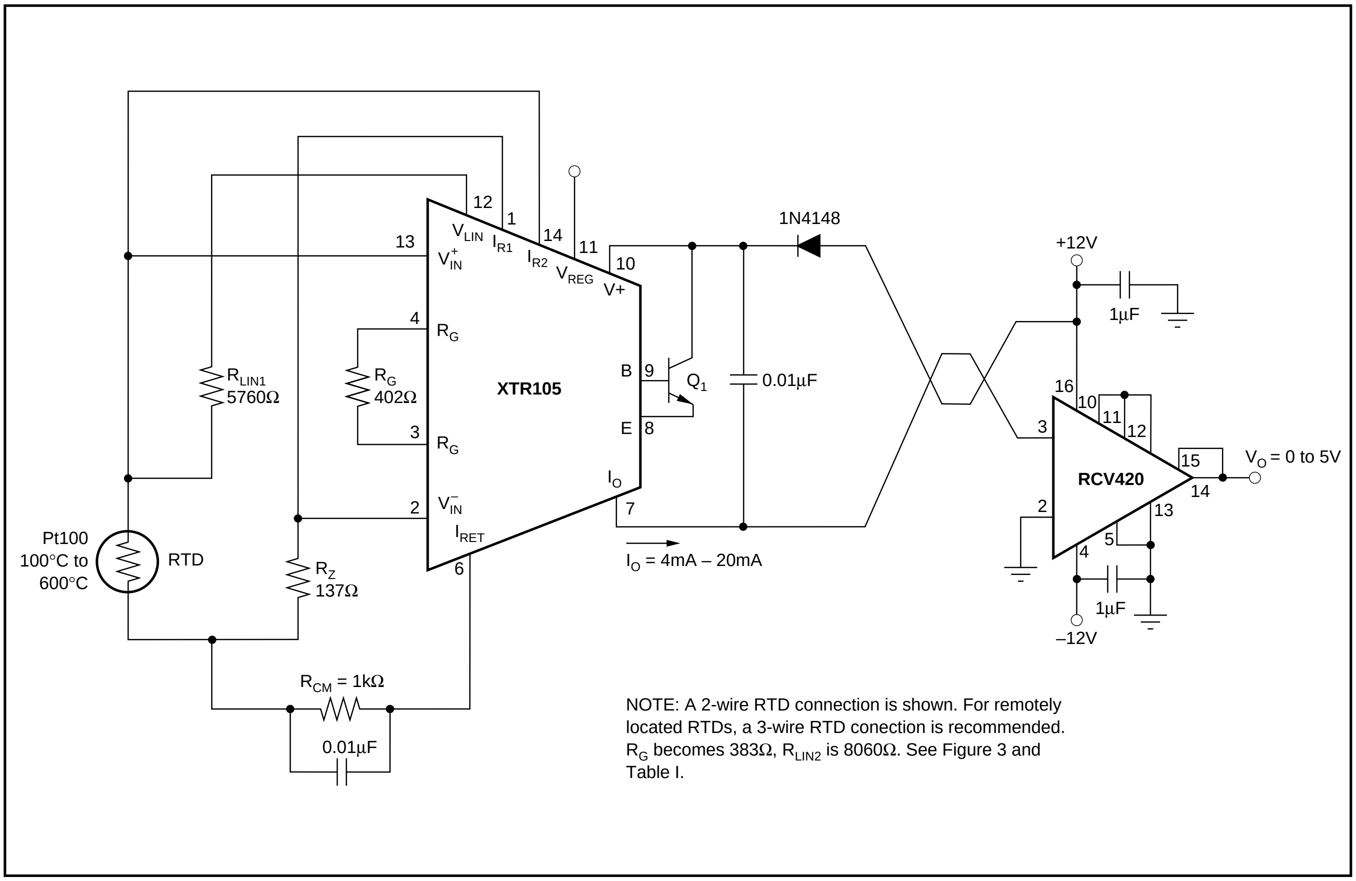


FIGURE 7. ±12V Powered Transmitter/Receiver Loop.

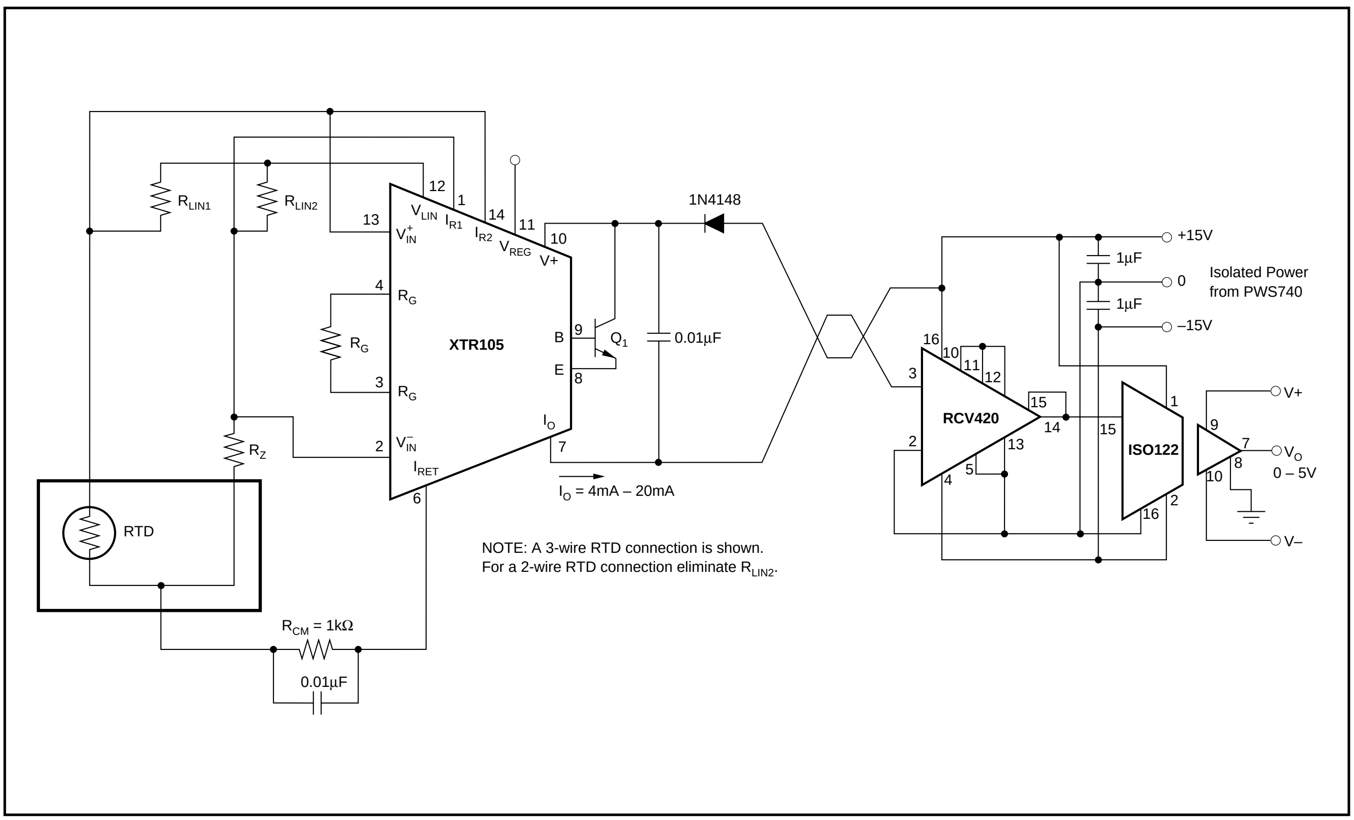


FIGURE 8. Isolated Transmitter/Receiver Loop.

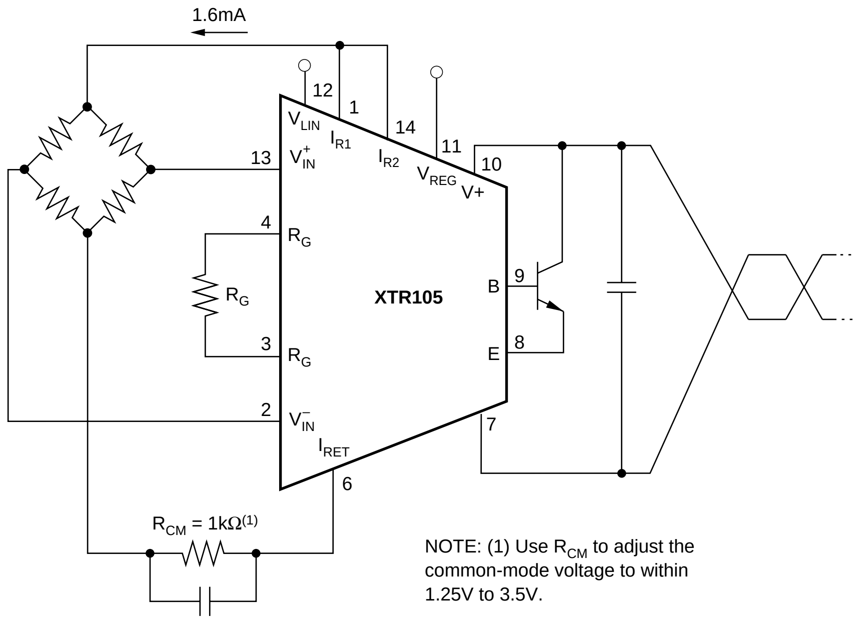


FIGURE 9. Bridge Input, Current Excitation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTR105P	ACTIVE	PDIP	N	14	25	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	XTR105P A	Samples
XTR105PA	ACTIVE	PDIP	N	14	25	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	XTR105P A	Samples
XTR105U	LIFEBUY	SOIC	D	14	50	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	XTR105U	
XTR105UA	LIFEBUY	SOIC	D	14	50	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	XTR105U A	
XTR105UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR105U A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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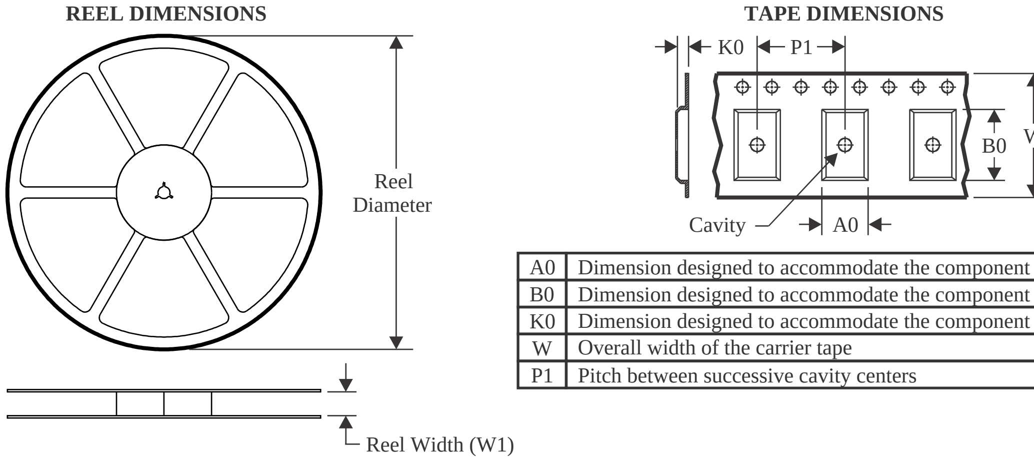
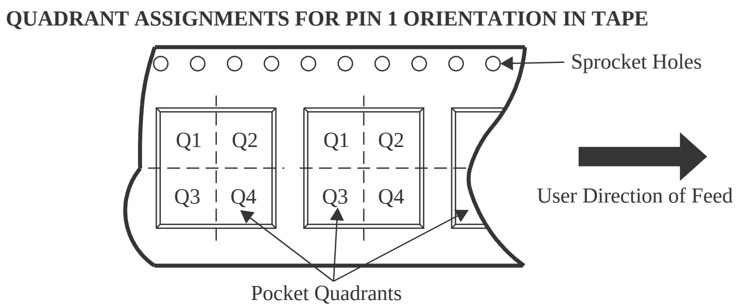
TAPE AND REEL INFORMATION



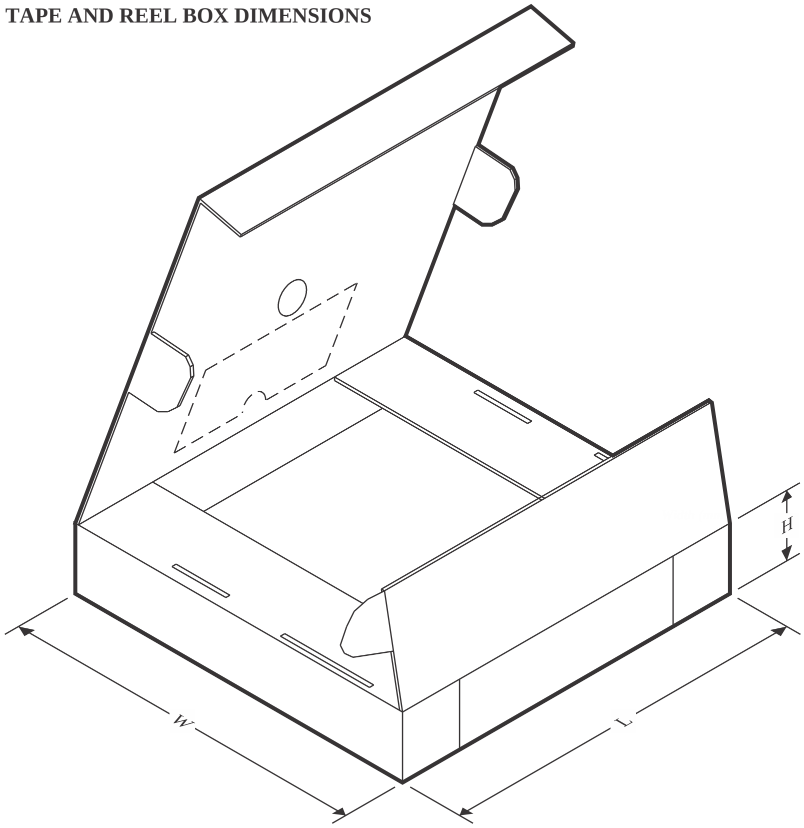
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR105UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

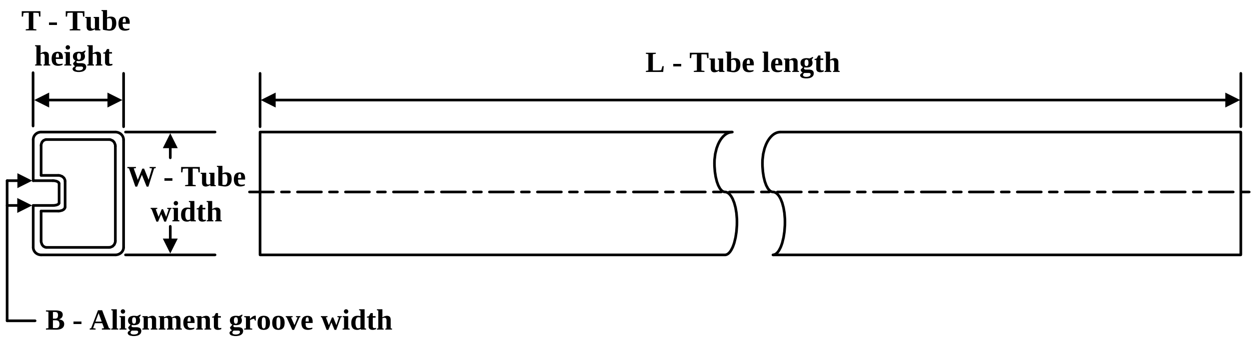
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR105UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0

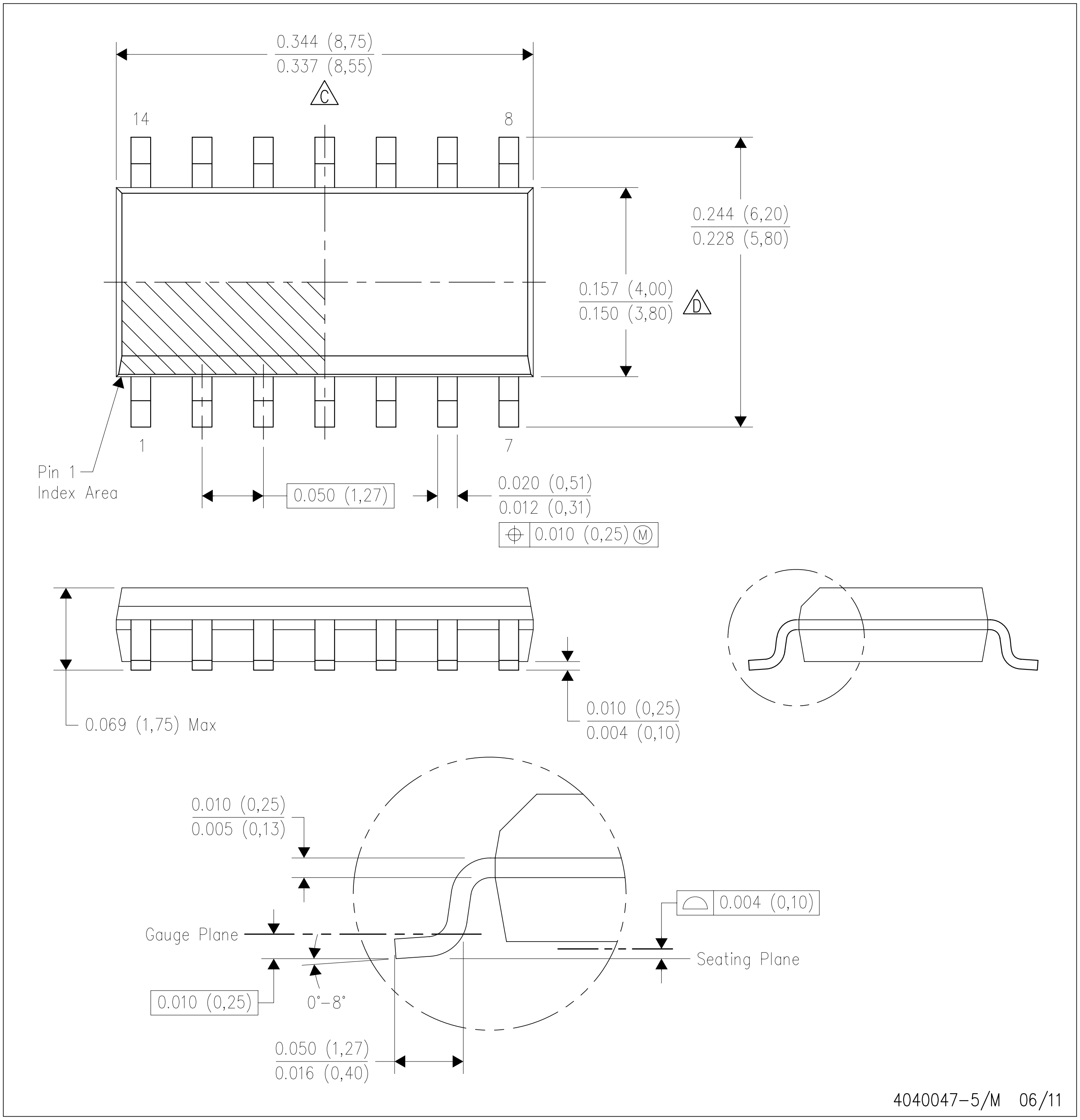
TUBE



*All dimensions are nominal

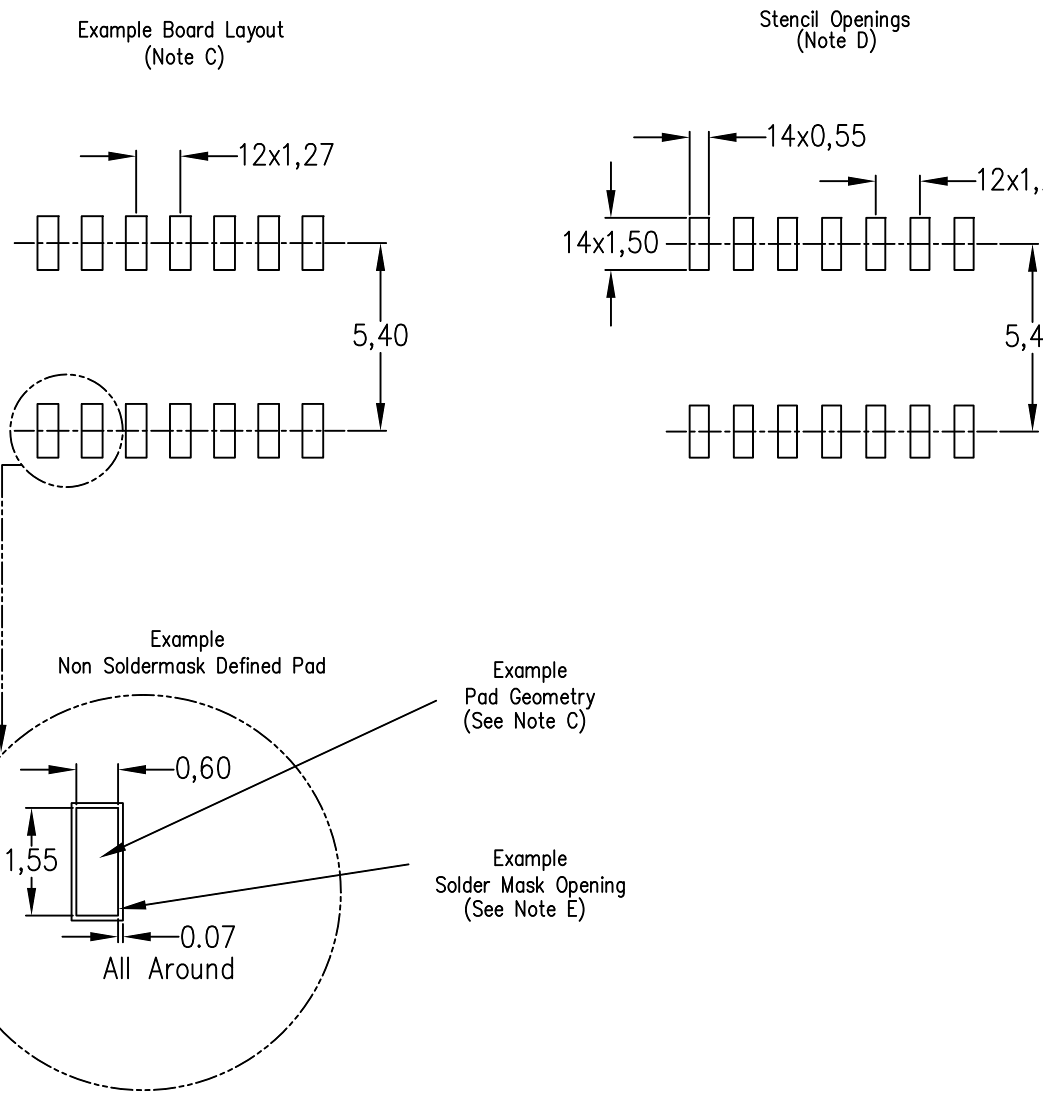
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
XTR105P	N	PDIP	14	25	506	13.97	11230	4.32
XTR105PA	N	PDIP	14	25	506	13.97	11230	4.32
XTR105U	D	SOIC	14	50	506.6	8	3940	4.32
XTR105UA	D	SOIC	14	50	506.6	8	3940	4.32

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE

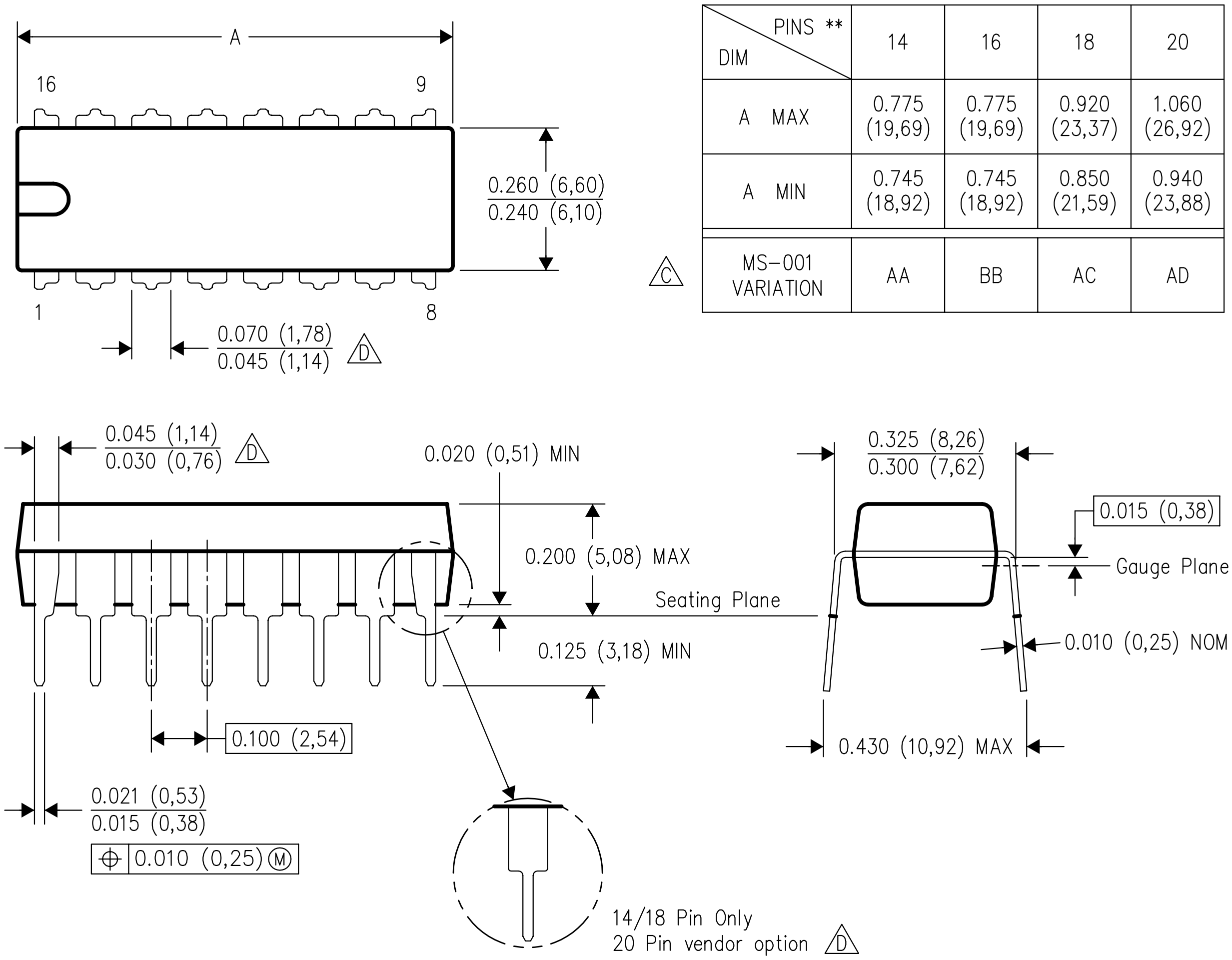


4211283-3/E 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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